Top-Gate GaN Thin-Film Transistors Based on AlN/GaN Heterostructures

Rongsheng Chen, Wei Zhou, Meng Zhang, and Hoi Sing Kwok

***Abstract*—Top-gate n-type GaN thin-film transistors (TFTs) based on AlN/GaN heterostructures were fabricated. GaN and AlN thin films were sequentially deposited by the reactive dc magnetron sputtering technique at room temperature on quartz. The proposed GaN TFTs exhibit good electrical performance, such as field mobility of 2.5 $cm^2/V \cdot s$, threshold voltage of 2.4 V, ON/OFF-current ratio of 1.2×10^5, and subthreshold swing of 0.5 V/dec. The proposed GaN TFT has great potential in the application of next-generation flat-panel displays.**

***Index Terms*—AlN, dc sputtering, GaN, thin-film transistors (TFTs).**

I. INTRODUCTION

BECAUSE of the superior transport properties of the 2-D electron gas (2DEG) channel, GaN-based high-electron mobility transistors are the focus of intense research activities in the area of high-power, high-speed, and high-temperature transistors [1]. The current deposition techniques for high-quality GaN-related thin films are mainly metal–organic chemical vapor deposition and molecular beam epitaxy. One of the current directions in GaN research is to deposit high-quality GaN thin films using inexpensive substrate under low temperature. Recently, amorphous and polycrystalline GaN thin films have been deposited using the magnetron sputtering technique [2]–[5] or the pulsed laser deposition technique [6]. The dc magnetron sputtering technique for the thin-film deposition has the potential of high deposition rate, large area, good uniformity, and low cost, suitable for mass production in the industry.

Transparent amorphous indium–gallium–zinc oxide thin-film transistors (TFTs) have become attractive for use as driving devices in large-scale active-matrix organic light-emitting diode applications, due to their higher mobility and larger area uniformity, as compared with amorphous and polycrystalline silicon TFTs [7], [8]. However, the poor electrical stability of ZnO-based TFTs is still a main issue in preventing commercialization [9]. Bottom- and top-gate-type TFTs using a reactive radio-frequency sputtering GaN thin film as a channel layer have been demonstrated and exhibited poor performance, such as low mobility (6×10^{-2} $cm^2/V \cdot s$) and low ON/OFF-current ratio (3×10^3) [10], [11]. We have reported that top-gate n-type GaN TFTs with a heavily doped source/drain region showed good electrical performance, such as high mobility ($1 cm^2/V \cdot s$) and high ON/OFF-current ratio (10^5) [12]. However, it needed high annealing temperature for the activation of the silicon dopant.

In this letter, as an alternative to ZnO-based TFTs, top-gate n-type GaN TFTs based on AlN/GaN heterostructures were fabricated. The properties of AlN thin films and the proposed GaN TFTs were studied and discussed in detail.

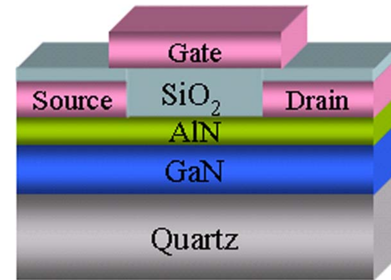

Fig. 1. Cross-sectional schematic of the proposed GaN TFT with a top-gate structure.

II. EXPERIMENTAL

The GaN thin films were deposited by reactive dc magnetron sputtering using a liquid gallium target at room temperature [12]. The AlN thin films were also prepared by the reactive dc magnetron sputtering technique using an aluminum target in mixed Ar and N_2 ambient ($Ar/N_2 = 1:1$) at room temperature. The deposition pressure and the input power for AlN thin films were 5 mtorr and 120 W, respectively. The structure of the films was analyzed by X-ray diffraction (XRD) experiments in grazing incidence geometry using Cu $K\alpha 1$ radiation at 40 kV, 40 mA. Atomic force microscopy (AFM) measurement was done in order to investigate the surface topography of the AlN thin films. The chemical composition of the AlN thin films was analyzed by X-ray photoelectron spectroscopy (XPS, Physical Electronics 5600 PHI) using an achromatic Mg $K\alpha$ X-ray source (1253.6 eV). XPS spectra were calibrated by the adventitious C 1s peak (285 eV) to compensate the charge effect.

The cross-sectional schematic of the proposed top-gate GaN TFTs in this letter is shown in Fig. 1. The process began with the standard RCA ($NH_4OH/H_2O_2/H_2O = 1/1/5$) cleaning of the quartz substrate (4 in in diameter, 0.5 mm in

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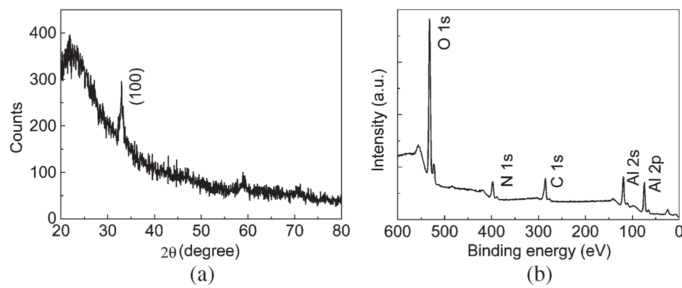

Fig. 2. (a) XRD pattern and (b) XPS spectra of the AlN thin film deposited at room temperature.

thickness). Then, the negative photoresist was coated, exposed with the active layer mask, and developed. After four cycles of deionized water spray rinse and bake, the substrate was transferred to a sputtering machine immediately. A 140-nm-thick GaN thin film as the active layer was first sputtered on the quartz substrate. Then, a 50-nm-thick AlN layer was sequentially sputtered on top of the GaN layer. The GaN and AlN layers were defined by the photolithography and liftoff process using one mask. The ohmic source/drain electrodes were formed by electron beam (e-beam) evaporation deposition of Ti/Al/Ni/Au (20 nm/150 nm/50 nm/80 nm), followed by rapid thermal annealing in N_2 ambient at 850 °C for 50 s. In order to eliminate the cracking problem of the thin films, the temperature ramp up is in three steps, i.e., from room temperature to 400 °C, 650 °C, and then 850 °C. The temperature ramp down is in reverse procedure. A 150-nm-thick SiO_2 layer, which was used as the gate dielectric, was deposited by plasma-enhanced chemical vapor deposition at 300 °C. Then, metal layers Ni/Au (50 nm/100 nm) were deposited as the gate electrode by e-beam evaporation and patterned by the photolithography and liftoff technique. The overlap length between the gate electrode and the source/drain contacts is 5 μm, as shown in Fig. 1. No further annealing treatment was needed in the process. The proposed GaN TFTs have a width-to-length ratio W/L of 2, with $L = 25$ μm. The electrical properties were measured at room temperature using an Agilent 4145B semiconductor parameter analyzer.

In order to investigate the operation mode of the proposed TFT device, three different types of capacitors were fabricated and measured, namely, Ti/AlN/SiO_2/Ni/Au (Capacitor A), Ti/GaN/SiO_2/Ni/Au (Capacitor B), and Ti/GaN/AlN/SiO_2/Ni/Au (Capacitor C). The process conditions were the same as those for the TFT devices. They were measured at a frequency of 10 kHz using an HP 4284A LCR meter.

III. Results and Discussion

Fig. 2(a) shows the XRD patterns of the AlN thin film deposited on quartz at room temperature. The strongest 2θ peak corresponding to (100) orientation was observed at 32.9°, indicating that the AlN thin film is polycrystalline with a wurtzite structure. Calculated from the Scherrer formula, the estimated average grain size of the deposited AlN thin film is about 4 nm. Fig. 2(b) shows an XPS broad spectrum of the deposited AlN films. Photoelectron peaks from aluminum, nitrogen, carbon, and oxygen can be seen. The carbon and oxygen contents were both attributed to the residual gas in the vacuum sputtering chamber and to the exposure of the films to air. The Al 2p peak at 74.1 eV and the N 1s peak at 397.3 eV reflect the N–Al chemical bonding in the sputtered AlN thin films. The relatively smooth surface, reasonably uniform, and ultrafine microstructure of the AlN thin films were confirmed by AFM measurement, as shown in Fig. 3. The root-mean-square roughness of the AlN thin film was only about 1 nm. Fig. 4 shows the normalized capacitance versus bias voltage characteristics of Capacitors A, B, and C. For Capacitor A, the capacitance does not vary with the bias voltage, which indicates no inversion or accumulation channel inside the AlN layer. Meanwhile, this constant capacitance does not indicate the existence of the 2DEG channel within the AlN layer. On the contrary, the variation of capacitance for Capacitors B and C indicates that the accumulation channel was at the SiO_2/GaN interface for Capacitor B or at the AlN/GaN interface for Capacitor C.

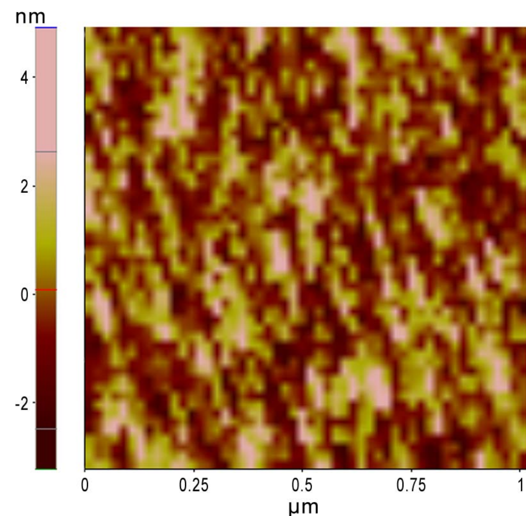

Fig. 3. AFM image for the polycrystalline AlN thin film.

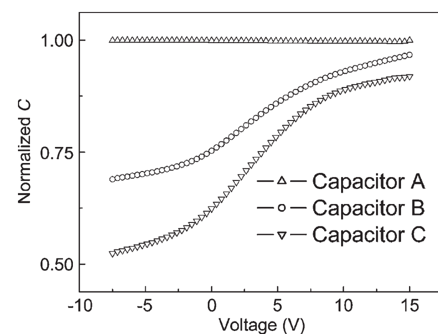

Fig. 4. Normalized C–V characteristics of Capacitors A, B, and C.

The typical output characteristics of this n-type GaN TFTs are shown in Fig. 5(a). Drain–source current I_{DS} exhibits pinchoff and saturation, indicating that the TFT follows standard field-effect transistor characteristics. I_{DS} of the GaN TFTs increased when a positive V_{GS} was applied. It indicates typical n-channel enhancement-mode characteristics. The output characteristic shows clear linear regions and does not show significant current crowding at low V_{DS}, indicating that low series resistance in source/drain contacts was obtained. This low

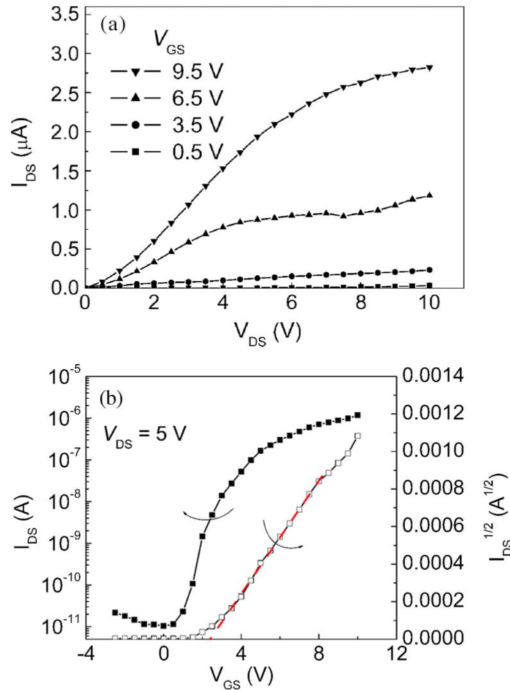

Fig. 5. (a) Output characteristics and (b) transfer characteristics of the proposed GaN TFTs (W/L = 50/25 μm).

series resistance was caused by the metal alloy Ti/Al/Ni/Au deposited by e-beam evaporation. Different from our previous report [12], no high-temperature and long-time annealing is needed for the activation of the silicon dopant in the source/drain region.

The saturation field-effect mobility is exacted with the devices operating in the saturation region, i.e.,

$$\mu_{\mathrm{FE}} = \frac{2L\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2}{WC_{\mathrm{OX}}}$$

where C_{OX} is the gate insulator capacitance per unit area, which is the same as that of Capacitor C ($\sim$17 nF/cm^2). The transfer characteristics with $V_{DS} = 5$ V for the GaN TFTs with the same channel width-to-length ratio are shown in Fig. 5(b). They exhibit good transfer TFT characteristics at a drain voltage of 5 V, such as saturation field-effect mobility of 2.5 cm^2/V $\cdot$ s, threshold voltage of 2.4 V, subthreshold swing of 0.5 V/dec, and ON/OFF-current ratio of 1.2×10^5. As compared with our previous report [12], this good performance of GaN TFTs studied in this letter may be enhanced by the 2DEG channel formed at the AlN/GaN heterointerface, which needs to be further investigated and demonstrated in the future.

IV. Conclusion

Good-performance top-gate n-type GaN TFTs based on AlN/GaN heterostructures have been fabricated in this letter. GaN and AlN thin films were deposited by dc reactive magnetron sputtering at room temperature in mixed Ar and N_2 ambient. Because of the metal alloy Ti/Al/Ni/Au for the source/drain ohmic contacts and the possibility of the 2DEG channel at the AlN/GaN heterointerface, the proposed GaN TFTs have saturation field-effect mobility of 2.5 cm^2/V $\cdot$ s, a threshold voltage of 2.4 V, a subthreshold swing of 0.5 V/dec, and an ON/OFF-current ratio of 1.2×10^5. The proposed top-gate GaN TFTs in this letter can be a potential candidate as driving devices in next-generation flat-panel displays.

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